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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): O. Inoue, et al.

Application No.: TBD

Filed: January 9, 2004

For: FABRICATION METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

Expected Group: 1756

Expected Examiner: C. Young

CLAIM FOR PRIORITY

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

January 9, 2004

Sir:

Pursuant to the provisions of 35 USC §119 and 37 CFR §1.55, Applicants hereby claim the right of priority based on Japanese Patent Application No. 2000-313513, filed in Japan on October 13, 2000.

A certified copy of the above-identified Japanese Patent Application was submitted on January 2, 2002, in prior Application No. 09/964,341, filed September 28, 2001.

Respectfully submitted,

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